REMARKS

Claims 17 - 23, 25, 26, 29 - 42, 46 - 48, and 52 - 65 have been amended. Claims 67 - 112 have been added. No claims have been canceled. Accordingly, Claims 17 - 23, 25 - 42, 44, 46 - 65, and 67 - 112 are now pending.

The claims have been revised to (a) format them in an internally consistent manner, (b) eliminate redundant language in several instances, (c) eliminate unnecessary punctuation, (d) clarify the grammar at various places, (e) make self-evident grammatical corrections in several instances, (f) make it clear that the second conductivity type is opposite to the first conductivity type, (g) make it clear that the "epitaxial" region in Claim 36 is the source region, (h) correct the dependencies of Claims 36, 40, and 61, (i) make it clear that the electrical contact in dependent Claim 64 is actually three electrical contacts, and (j) correct "semiconductor body" to "body region" in Claim 65. Aside from the claim dependency corrections and the correction to Claim 65, the revisions to the claims do not, as far as Applicants' attorney is aware, change the scope of any of the previously pending claims. Nor is any of the claim revisions being made to distinguish any prior art document or in response to any rejection.

The application is ready for continued examination in light of the accompanying Information Disclosure Statement.

Please telephone Applicants' attorney at 408-453-9200, ext. 1371, if there are any questions.

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APPENDIX

AMENDED CLAIMS 17 - 23, 25, 26, 29 - 42, 46 - 48, AND 52 - 65, WITH ANNOTATIONS TO INDICATE REVISIONS, AND UNCHANGED CLAIMS 27, 28, 44, AND 49 - 51 OF U.S. PATENT APPLICATION 08/851,608, ATTORNEY DOCKET NO. M-799-4C US

17. (Four times amended) A trench DMOS transistor cell[,] comprising:

a substrate of a first conductivity type, said substrate having a surface;

an epitaxial layer of said first conductivity type formed on said surface of said substrate, said epitaxial layer having a top surface and a bottom surface, said epitaxial layer having a substantially uniform initial dopant concentration at formation;

a body region of a second conductivity type opposite to said first conductivity type formed in said epitaxial layer, said body region extending, as measured from said top surface of said epitaxial layer, to a first depth d_{max} at a first location and to a depth [of] d at a second location, where d is less than d_{max}, said first and second locations being separated by a predetermined horizontal distance;

a source region of said first conductivity type formed in said expitaxial layer above a portion of said body region, said portion of said body region being located between said second location and said source region; and

a trench formed in said epitaxial layer, having substantially vertical side walls, and extending from said top surface of said epitaxial layer to a depth d_{tr}[, said depth d_{tr} being] less than said depth d_{max}[,] and greater than said depth d, said trench being (i) closer to said second location than to said first location[,] and (ii) horizontally adjacent to said source region; wherein breakdown in said trench DMOS transistor cell occurs across said epitaxial layer at a position closer to said first location than to said second location.

18. (Amended) A trench DMOS transistor cell as in Claim 17[,] wherein said body region has a portion exposed at said top surface of said epitaxial layer.

19. (Amended) A trench DMOS transistor cell as in Claim 18[,] wherein said source region has a portion exposed at said top surface of said epitaxial layer.

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20. (Twice amended) A trench DMOS transistor cell as in Claim 17[,] wherein depth d_{tr} is less than d_{max} by an amount sufficient to cause semiconductor surface breakdown to occur at a location closer to said first location than to said second location.

21. (Twice amended) A trench DMOS transistor cell as in Claim 17[,] wherein said epitaxial layer has a thickness d_{epi} small enough to cause semiconductor surface breakdown to occur at a location closer to said first location than to said second location.

22. (Amended) A trench DMOS transistor cell as in Claim 17[,] wherein said trench, when viewed from above said top surface of said epitaxial structure, is polygonal and has [, having] a number of sides greater than four.

23. (Amended) A trench DMOS transistor cell as in Claim 22[,] wherein said number of sides is six.

25. (Amended) A trench DMOS transistor cell as in Claim 17[,] wherein said trench contains [comprises] polysilicon isolated from said source and body regions by a layer of gate oxide.

26. (Twice amended) A trench DMOS transistor cell as in Claim 21[,] wherein said gate oxide has [having] a thickness sufficient to cause semiconductor breakdown to occur at a location closer to said first location than to said second location.

27. (Unchanged) A semiconductor wafer comprising a predetermined number of trench DMOS transistor cells in an closed cell configuration, each trench DMOS transistor cell in said semiconductor wafer being a DMOS trench transistor cell as recited in Claim 17.

28. (Unchanged) A semiconductor wafer comprising a predetermined number of trench DMOS transistor cells in an open cell configuration, each trench DMOS transistor cell in said semiconductor wafer being a DMOS trench transistor cell as recited in Claim 17.

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29. (Twice amended) A trench DMOS transistor cell as in Claim 17[,] wherein said substrate has a dopant concentration higher than said initial dopant concentration of said epitaxial layer, said substrate and said epitaxial layer forming respectively drain and drift regions of said trench DMOS transistor cell.

30. (Four times amended) A trench DMOS transistor cell[,] comprising:

a substrate of semiconductor material of a first electrical conductivity type having a top surface;

a first covering layer of semiconductor material of said first electrical conductivity type, said first covering layer (i) having a dopant concentration less than that of said substrate, (ii) having a top surface and (iii) being contiguous to and overlying the [substrate] top surface of the substrate;

a second covering layer of semiconductor material of a second electrical conductivity type opposite to said first electrical conductivity type having a top surface and being contiguous to the top surface of the first covering layer and extending vertically downward from the top surface of the first covering layer into an upper portion of the first covering layer;

a third covering layer of semiconductor material of said first electrical conductivity type having a top surface and being contiguous to and partly overlying the top surface of the second covering layer[,] where the maximum depth of the second covering layer relative to the top surface of the third covering layer is a depth d_1;

a trench, having side walls and a bottom wall, said side walls extending vertically downward from the top surface of the third covering layer through the third and second covering layers and through a portion of, but not all of, the first covering layer, where the trench has a maximum depth relative to the top surface of the third covering layer equal to a second depth d_2 [and d_2 is] less than d_1;

a layer of oxide positioned within the trench and contiguous to the bottom walls and side walls of the trench so that portions of the trench are filled with the oxide layer;

electrically conducting semiconductor material[,] contiguous to the oxide layer and positioned within the trench so that the oxide layer lies between the electrically conducting semiconductor material and the bottom and side walls of the trench; and

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three electrodes [that are] electrically coupled to the electrically conducting semiconductor material in the trench, to the third covering layer and to the substrate, respectively; wherein junction breakdown occurs away from the trench and into a portion of the second covering layer.

31. (Twice amended) A trench DMOS transistor cell as in Claim 30[,] wherein said trench comprises rounded edges of oxidized material.

32. (Thrice amended) A trench DMOS transistor cell[,] comprising:

a substrate;

an epitaxial layer above the substrate;

a trench in the epitaxial layer, the trench having substantially vertical side walls and having a predetermined depth d_{tr}; and

a body region in the epitaxial layer, the body region having a predetermined maximum depth d_{max}; wherein [the] depth d_{tr} is less than [the] depth d_{max}, and wherein junction breakdown occurs away from the trench and into the epitaxial layer.

33. (Amended) A trench DMOS transistor cell as in Claim 32[,] wherein the substrate is of a first conductivity type, the epitaxial layer is of said first conductivity type and the body region is of a second conductivity type opposite to said first conductivity type.

34. (Amended) A trench DMOS transistor cell as in Claim [claim] 33 wherein the epitaxial layer has a top surface and the body region extends from the epitaxial layer's [layer] top surface into an upper portion of the epitaxial layer.

35. (Amended) A trench DMOS transistor cell as in Claim [claim] 34 wherein a source region is formed in said epitaxial layer.

36. (Twice amended) A trench DMOS transistor cell as in Claim 35 [34] wherein the source [an epitaxial] region partially covers the body region.

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37. (Twice amended) A trench DMOS transistor cell as in Claim 36 wherein the body region includes a heavily doped portion [body region] extending upward through the epitaxial region and forming a [an exposed] pattern at the epitaxial layer's [layer] top surface.

38. (Amended) A trench DMOS transistor cell as in Claim 37 wherein the trench laterally surrounds the [exposed] pattern of the heavily doped portion of the body region.

39. (Amended) A trench DMOS transistor cell as in [of] Claim 32 further comprising [wherein the trench has side walls, said DMOS transistor cell having] an oxide layer on said trench side walls, [; and wherein] said oxide layer having [is etched to create] rounded corners along [in] said trench.

40. (Amended) A trench DMOS transistor cell as in Claim 32 [39,] further comprising a gate oxide layer within the trench.

41. (Twice amended) A trench DMOS transistor cell as in [of] Claim 40 further comprising electrically conducting material contiguous to the gate oxide layer, [wherein] the gate oxide layer being [is] located between the electrically conducting material and the trench.

42. (Thrice amended) A trench DMOS transistor cell as in Claim 40[,] further comprising:

a first polysilicon layer on a portion of said gate oxide layer;

a second oxide layer on a portion of said first polysilicon layer;

a second polysilicon layer on a portion of said second oxide layer; and

a metal layer wherein said first polysilicon layer extends from the trench to a field region creating an electrical contact to the metal layer and providing continuity from the metal layer to the trench.

44. (Unchanged) A trench DMOS transistor cell as in Claim 32 wherein a horizontal cross section of the cell has a polygonal shape.

46. (Twice amended) A transistor[,] comprising:

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a first region of a first conductivity type;

a second region of a second conductivity type opposite to the first conductivity type overlying [over] said first region;

a third region of said first conductivity type such that said first and third regions are separated by said second region;

a trench[,] having substantially vertical side walls and [,] extending through said third and second regions; and

a gate in said trench; wherein a portion P of said second region, which portion P is spaced from said trench, extends deeper than said trench so that, if a predetermined voltage is applied to said gate and to said third region and another predetermined voltage is applied to said first region, [an] avalanche breakdown occurs away from a surface of said trench.

47. (Amended) A transistor as in Claim [claim] 46 wherein said portion P of said second region is more heavily doped [heavier] than another portion of said second region [which portion is] adjacent to said trench.

48. (Amended) A transistor as in Claim 46 wherein said first region comprises a first portion and a second portion over said first portion, said second portion being more lightly [lighter] doped than said first portion.

49. (Unchanged) A transistor as in Claim 48 wherein said avalanche breakdown is a reach-through breakdown across said second portion.

50. (Unchanged) A transistor as in Claim 46 wherein said portion P of said second region extends deeper than said trench by more than 0.5 μm.

51. (Unchanged) A transistor as in Claim 46 further comprising an insulator between said surface of said trench and said gate.

52. (Twice amended) A transistor[,] comprising:

a first region of a first conductivity type;

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a second region of said first conductivity type over said first region, said second region being more lightly [lighter] doped than said first region;

a third region of a second conductivity type opposite to the first conductivity type overlying [over] said second region, said second and third regions forming a junction;

a fourth region of said first conductivity type over said third region;

a trench[,] having substantially vertical side walls and[,] extending through said fourth and third regions; and

a gate in said trench; wherein a deepest part of said third region is laterally spaced from said trench; and wherein a distance between said deepest part of said third region and said first region is less than a depletion width of a planar junction which has the same doping profile as does said junction between said second and third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage.

53. (Twice amended) A transistor as in Claim [claim] 52 wherein the deepest of said third region is doped more heavily [heavier] than a part of said third region [which part is] adjacent to said trench.

54. (Thrice amended) A semiconductor device comprising[:] a semiconductor structure having a trench therein of depth d_{tr} and substantially vertical side walls, said semiconductor structure including a drain region, a source region, a body region, and a gate region within said trench and separated from said body region by [a] dielectric material, said body region having a maximum depth [of] d_{max}[, wherein said maximum depth d_{max} being] greater than said depth d_{tr}, [and] wherein junction breakdown occurs away from said trench.

55. (Amended) A semiconductor device as in Claim 54[,] further comprising a substrate of a first conductivity type[,] and an overlying epitaxial layer of said first conductivity type, [and] wherein said body region is of a second conductivity type opposite to said first conductivity type.

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56. (Thrice amended) A semiconductor device as in Claim [claim] 55 wherein the epitaxial layer has a top surface and the body region extends from a surface of the epitaxial layer into an upper portion of the epitaxial layer.

57. (Amended) A semiconductor device as in Claim [claim] 55 wherein a source region is formed in said epitaxial layer.

58. (Four times amended) A semiconductor device as in Claim 55 wherein said body region extends upward through the epitaxial layer and forms a [forming an exposed] pattern at a surface of said epitaxial layer.

59. (Amended) A semiconductor device as in Claim 58 wherein the trench laterally surrounds the [exposed] pattern of the body region.

60. (Amended) A semiconductor device as in Claim 54 further comprising [wherein said trench has side walls, said semiconductor device having] an oxide layer on said trench walls, [and wherein] said oxide layer having [is etched to create] rounded corners along [in] said trench.

61. (Amended) A semiconductor device as in Claim 54 [60,] further comprising a gate oxide layer within the trench.

62. (Amended) A semiconductor device as in Claim 61 further comprising [an] electrically conducting material contiguous to said gate oxide layer, wherein said gate oxide layer is located between said electrically conducting material and said trench.

63. (Twice amended) A semiconductor device as in Claim 61[,] further comprising:

a first polysilicon layer on a portion of said gate oxide layer;

a second oxide layer on a portion of said first polysilicon layer;

a second polysilicon layer on a portion of said second oxide layer; and

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a metal layer wherein said first polysilicon layer extends from the trench to a field region creating an electrical contact to the metal layer and providing continuity from the metal layer to the trench.

64. (Twice amended) A semiconductor device as in Claim 54[,] further comprising three [an] electrical contacts [contact] respectively to the gate region, the drain region, and simultaneously to the body region and the source region.

65. (Amended) A semiconductor device as in Claim 54 wherein a horizontal cross section of said [semiconductor] body region has a polygonal shape.

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